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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/870,944	06/01/2001	Michael I. Catherwood	18153.0040	8704

31625 7590 04/21/2006

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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2193	

DATE MAILED: 04/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/870,944	CATHERWOOD, MICHAEL I.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/15/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 02/15/2006.

2. Claims 1 and 3-5 are pending in this application. Claim 1 is independent claims. In Amendment, claims 2 and 6-7 are cancelled. This Office Action is made final.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 and 3-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Ishida et al. (U.S. 4,945,507).

Re claim 1, Ishida et al. disclose in Figures 1-2 a system for overflow (e.g. 34 as overflow detection and prevention) and saturation processing (e.g. 28, 32, 22 in Figure 1 as saturation selection operands) comprising: an adder (e.g. 10), operatively connected to receive first (e.g. 12) and second operands (e.g. 16), and connected to add the operands to produce a result of the added operands (e.g. 22); an accumulator (e.g. 46), operatively connected to store at least a portion of the result of the added operands (e.g. least 20 bits input into 48) or at least a portion of a selected one of predetermined constants (e.g. from either 28 or 32 when saturate encountered) based on control signals (e.g. 42 and 40);

guard bits (e.g. D22 and D23 in Figure 2), operatively connected to store the remaining portion of the result of the added operands (e.g. the most significant bits of output of adder 10) or the remaining portion of the selected one of predetermined constants based on the control signals (e.g. when feedback of accumulate); overflow logic (e.g. 34) operatively connected to the accumulator and to the guard bits so as to indicate overflow of the accumulator (e.g. output of 34 as 42 and 40); and saturation logic (e.g. 28, 32, 22, and 24), operatively connected to the adder (e.g. 10), to the guard bits (e.g. Figure 2), and connected to provide the control signals based on at least a portion of the result of the added operands and at least a portion of the guard bits (e.g. Figure 2); and logic means (e.g. Figure 2 particularly 66) for comparing most significant bits of the guard bits and most significant bit of the result of the added operands and for generating the control signals (e.g. 42 and 40) in accordance with the comparison.

Re claim 3, Ishida et al. further disclose in Figures 1-2 the saturation logic includes a selector (e.g. 24) operatively connected to selectively provide a one of the result of the added operands or a one of the predetermined constants based on the comparison (e.g. either from 28, 32, or 22).

Re claim 4, Ishida et al. further disclose in Figures 1-2 the logic means includes means (e.g. 34) for providing the control signals in accordance with an enable signal and in accordance with the comparison (e.g. 42 and 40).

Re claim 5, Ishida et al. further disclose in Figures 1-2 the logic means responsive to the comparison (e.g. 34 and Figure 2 in particular with part 66), for selectively providing the control signals (e.g. 42 or 40) so that the accumulator stores at least a

portion of the result of the added operands and the guard bits store the remaining portion of the result of the added operands (e.g. if no overflow), or the accumulator stores at least a portion of a predetermined constant and the guard bits store the remaining portion of the predetermined constant (e.g. otherwise the content of either 28 or 32 is stored depending on the direction control signal).

Response to Arguments

5. Applicant's arguments filed 02/15/2006 have been fully considered but they are not persuasive.

a. The applicant argues in pages 5-6 for claim 1 that the cited reference by Ishida et al. fails to disclose guard bits, operatively connected to store the remaining portion of the result of the added operands or the remaining portion of the selected one of predetermined constants based on the control signals as cited in the claimed.

The examiner respectfully submits that the cited reference discloses either inherently or expressively all the elements in claim 1. Generally, the most significant bit(s) of adder 10 are considered as the guard bit(s), which is stored in flip-flop register 62 in Figure 2 or 6. This portion of the result is used to determined the overflow detection and select the correct result for storing base on the overflow detection.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

April 12, 2006

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100